

Department of Electrical and Computer Engineering
The Robotics Institute

Metrology Systems Perspective on Micro/Nano Devices

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***NIST Workshop on Metrology Needs for
Micro/Nano-Technology
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MEMS Metrology

■ Dimensions

- displacements, modes
- widths, gaps
- sidewalls, underwalls
- roughness
- curling, shape

■ Material properties

- E , ν
- stress, stress gradients
- density
- damping
- thermal properties
- active properties

■ Tribology

- Friction, Stiction
- Creep
- Wear
- Fatigue
 - static / dynamic

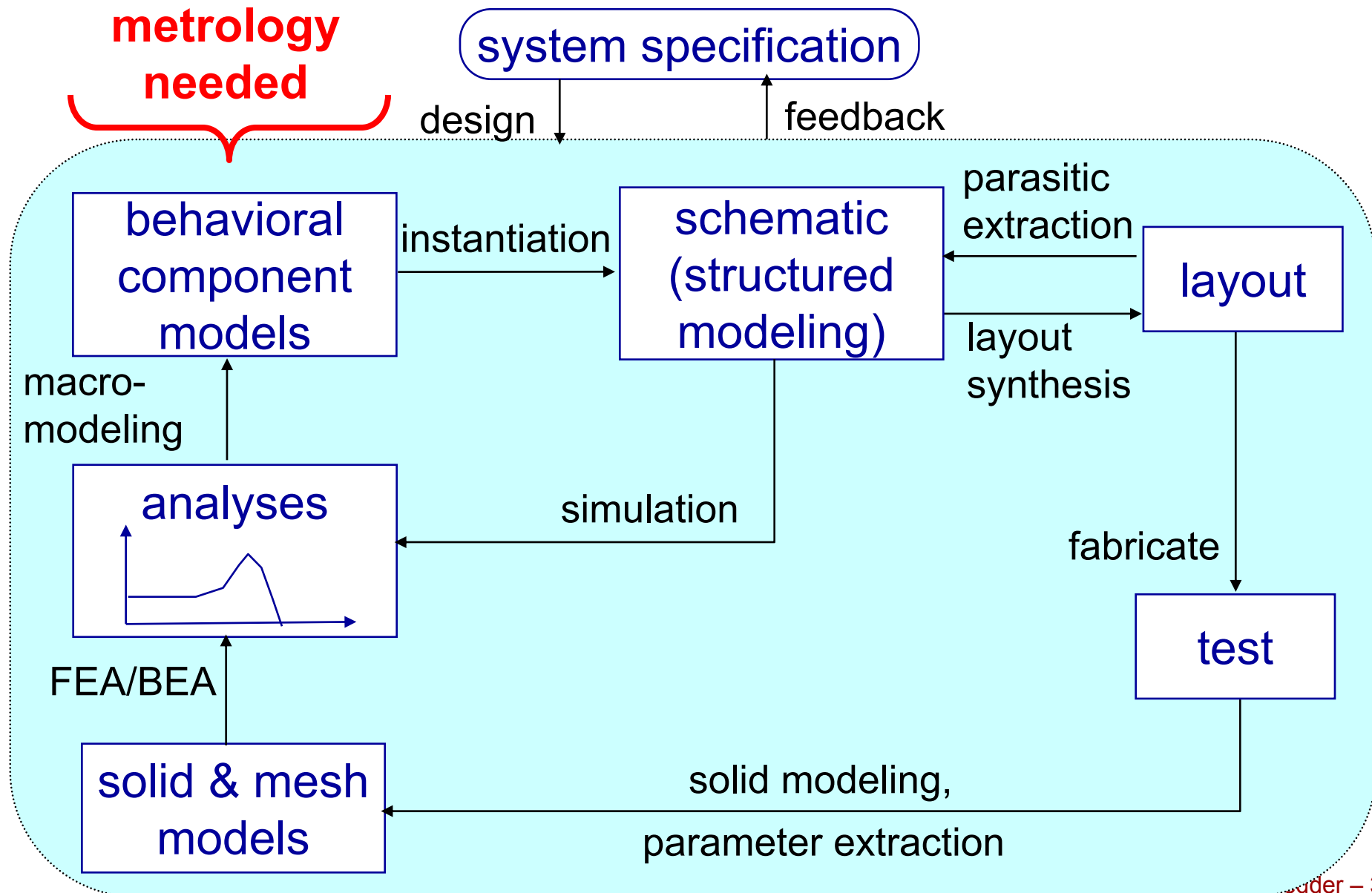
■ Yield

- defects
- faults

■ Variation

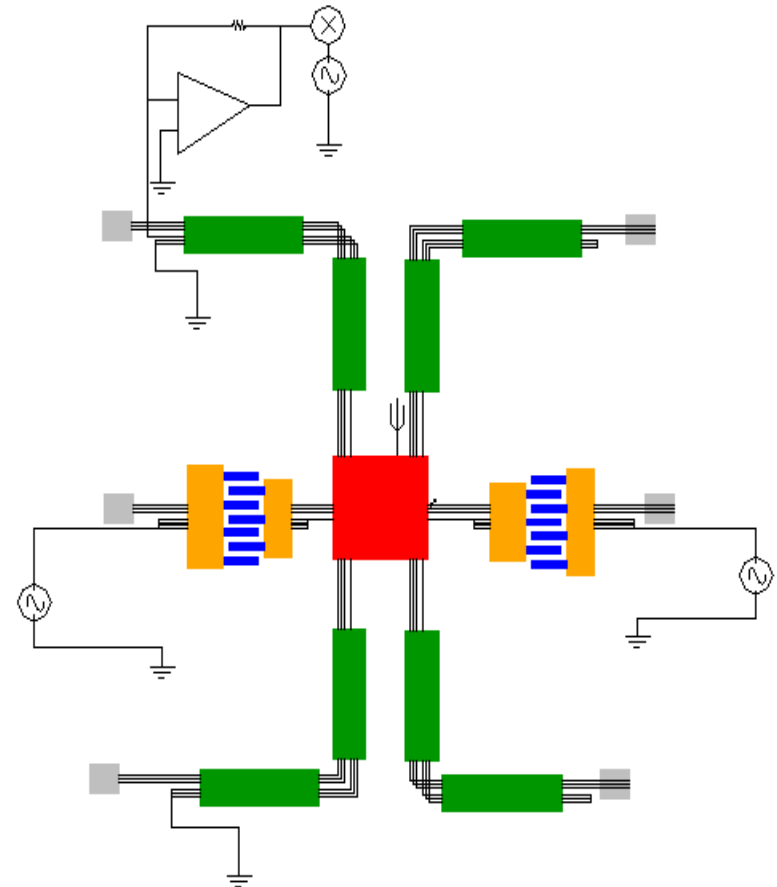
- temperature
- die to die variation
- run to run variation
- aging
- packaging
- ambient

MEMS Design Flow



MEMS Circuit Schematic

- Schematic composition of behavioral models
- Tools:
 - MEMSCAP's MEMSPro
 - Coventor's ARCHITECT
 - UC Berkeley's SUGAR
 - Carnegie Mellon's NODAS



MEMS Design Testbed Vision

- Driven by MEMS Schematic/Simulation Design Tools
-
- Flow A) MEMS metrology system
 - Extract structure (size and defects)
 - Generate solid model and mesh
 - Back annotate to MEMS schematic
- Flow B) MEMS Automated Testbed
 - Design and simulate microstructures
 - Download testbed configuration to Microvision system
 - Compare simulated and measured results

Automated Testbed Data Flow

*Process material properties:
 E , ρ , TCE , thickness, σ*

*Stimulus,
 outputs*

Test equipment

Microvision
 system

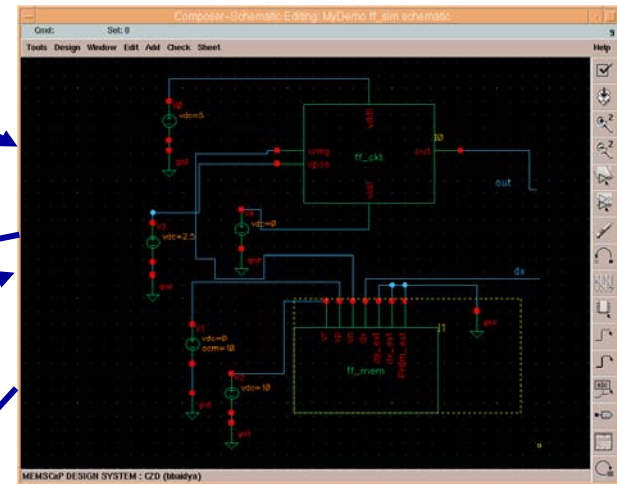
x-y drive

Image
 registration

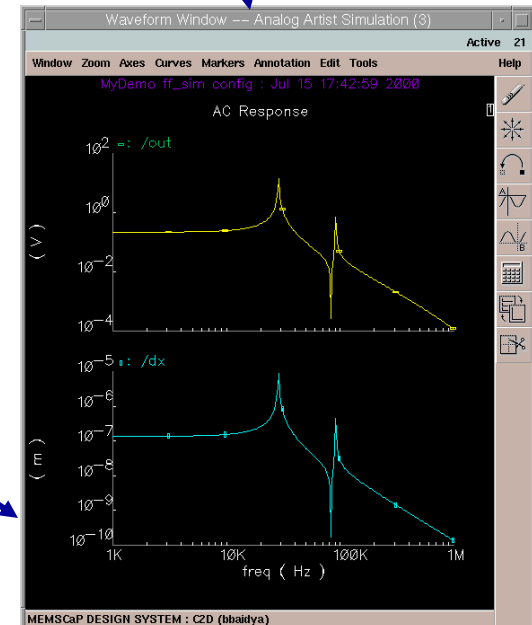
*Extracted
 geometry*

*Layout,
 nodes*

measurements



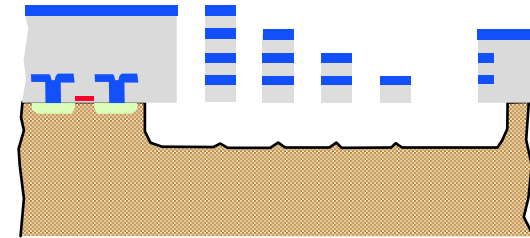
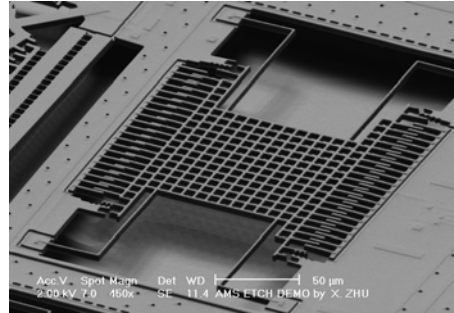
simulation



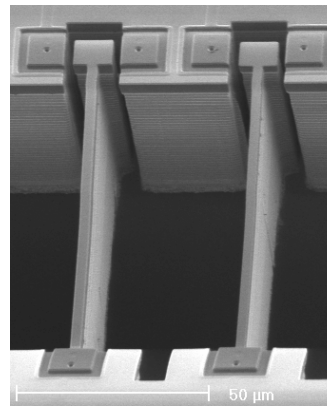
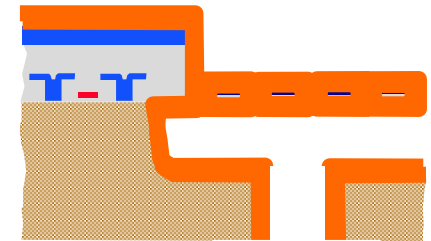
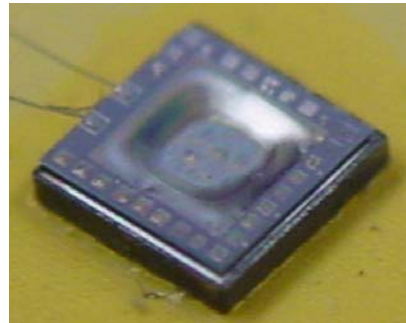
CMOS-MEMS Technologies

- Foundry process technology base
 - Highly integrated microsystem platforms
 - But, MEMS material properties are not quantified
- Questions always asked:
 - How reliable?
 - What is variation to “X”?
- Requires LOTS of samples and measurements
 - time, effort and \$

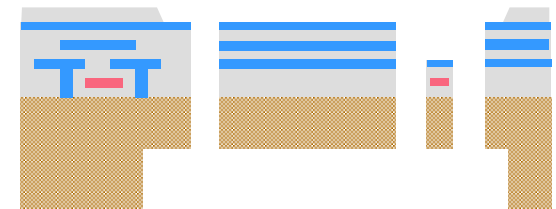
Thin-Film CMOS-MEMS



Membrane CMOS-MEMS



DRIE Si CMOS-MEMS



Geometry Example: CMOS MEMS Beams

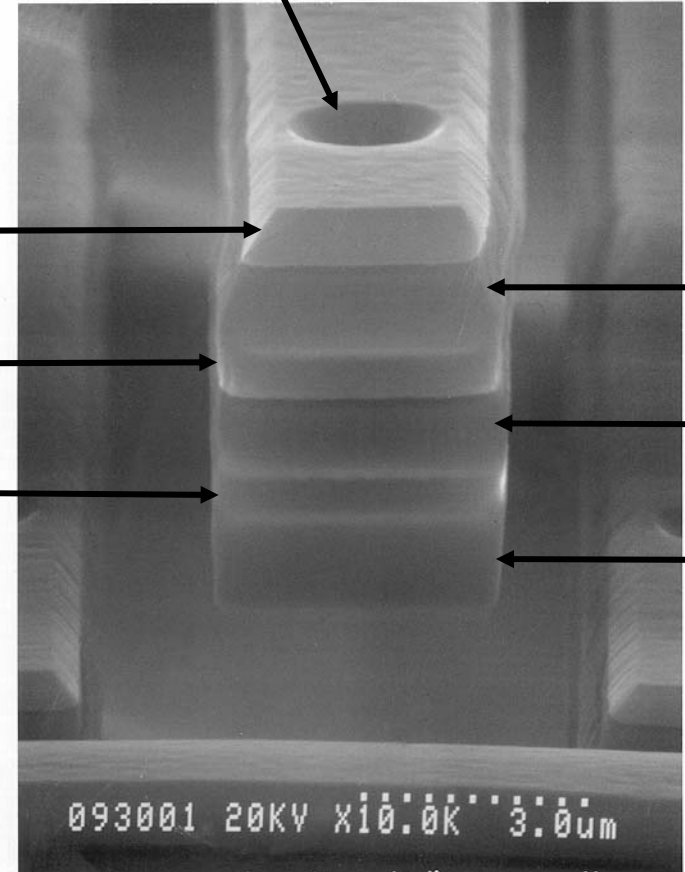
- Top metal is exposed and thinned by ion milling
- Underlying metal layers may be exposed, depending on layout

Via from Metal-3 to Metal-2

Metal-3

Metal-2

Metal-1



Oxide layers

Process & DRC Test Structures

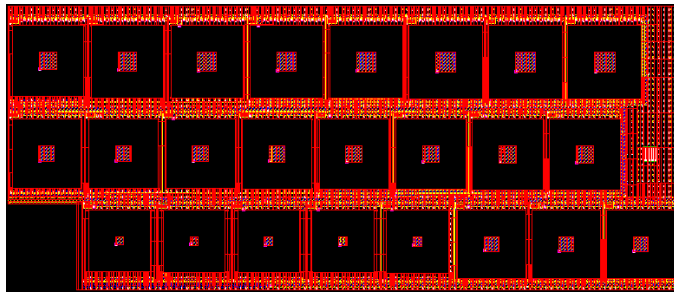
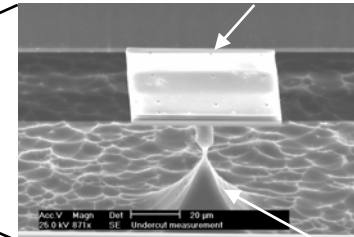
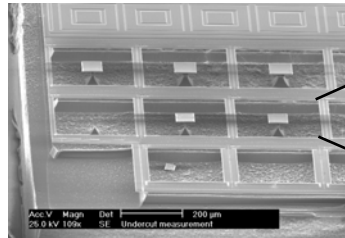


Plate with no Holes Undercut Test



CMOS-MEMS Plate

Si undercut

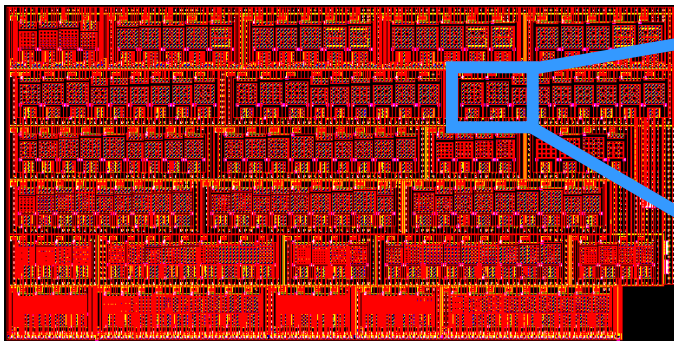
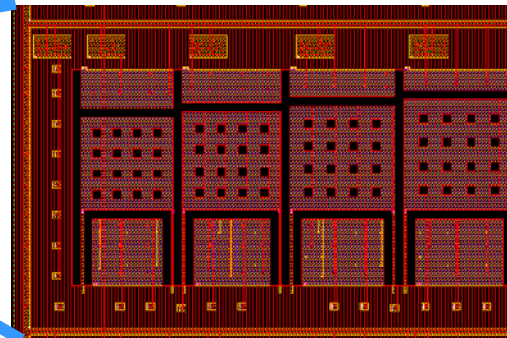
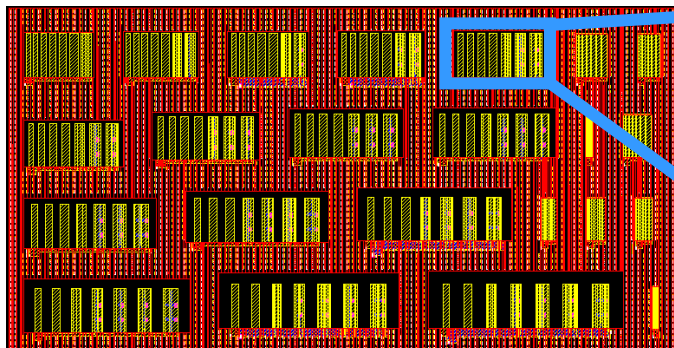


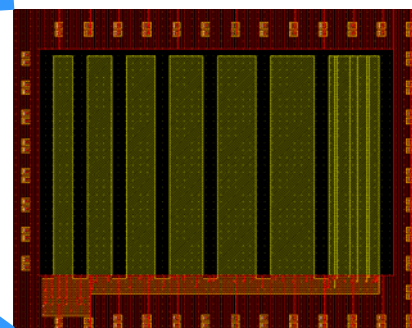
Plate With Holes Release DRC



6 μm gap
6 μm x 6 μm holes
{60.5, 64.5, 68.5,
72.5} μm plate width



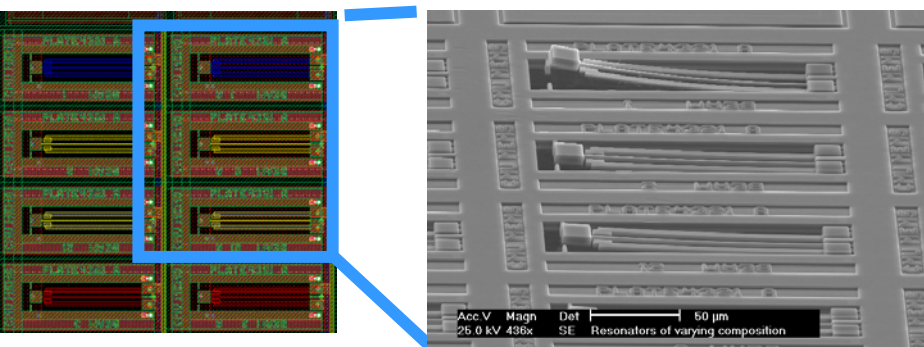
Beam Release DRC



10 μm gap
{13.0, 16.6, 19.5, 22.5,
26.3, 30.0, 34.2} μm
beam widths

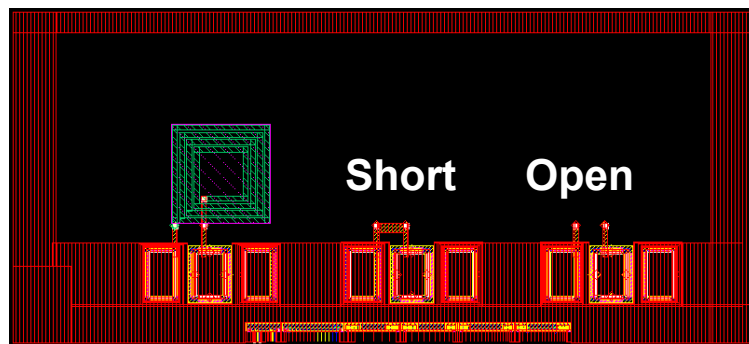
Material & Device Test Structures

Mechanical properties:



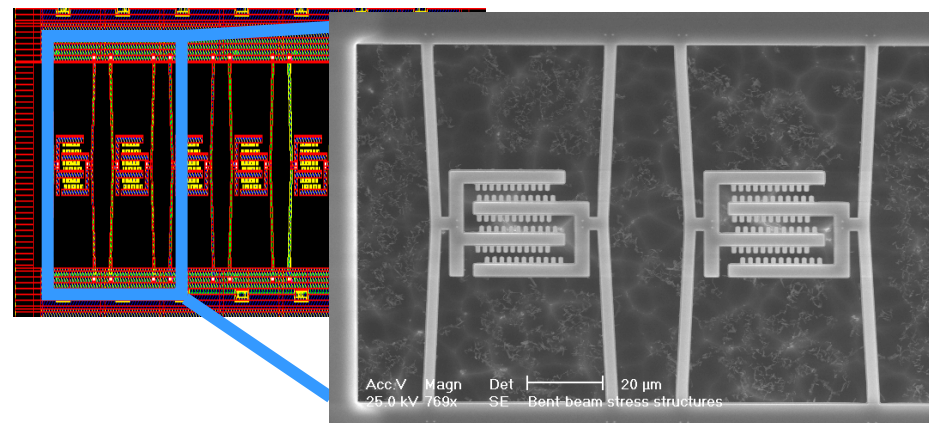
Beam Resonator
Length $125\ \mu\text{m}$
Plate $15\ \mu\text{m} \times 15\ \mu\text{m}$

RF-MEMS passives:



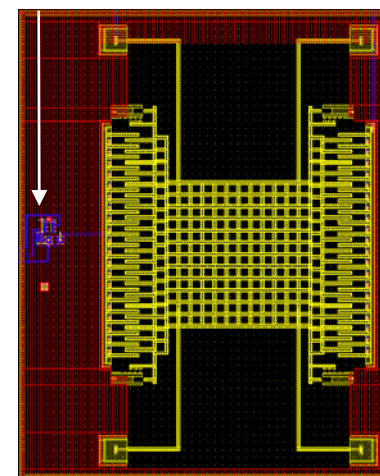
Inductor

Axial Stress



Capacitive interfaces:

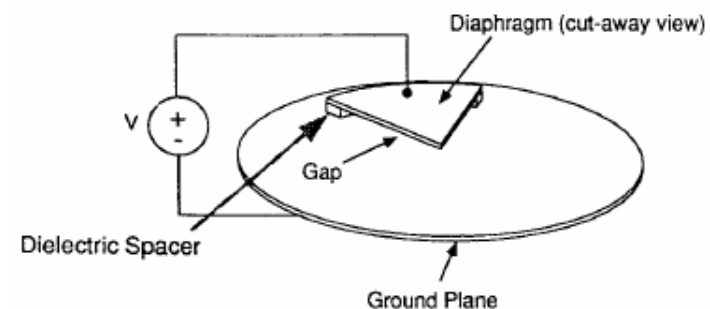
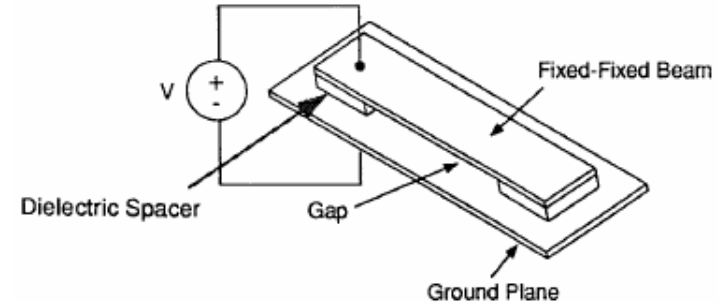
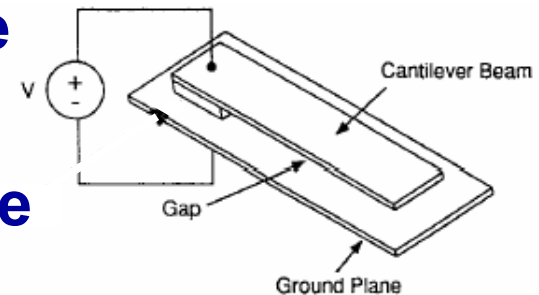
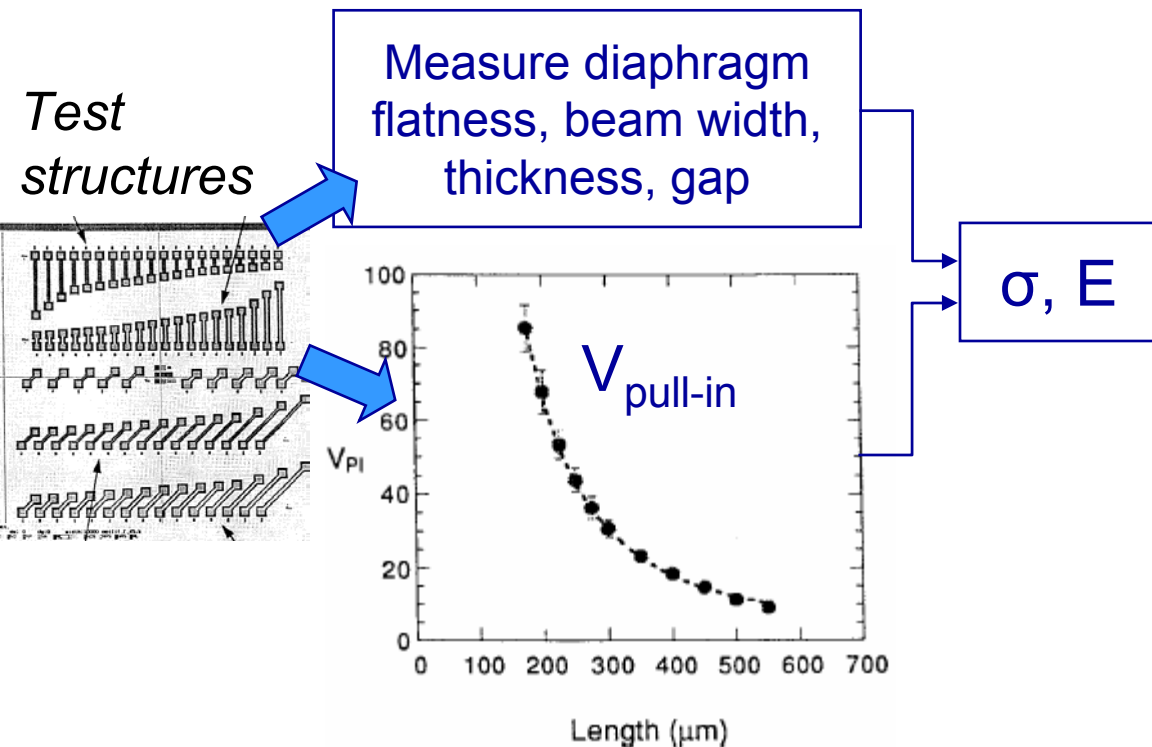
Output Buffer Amp



Crab-leg Resonator

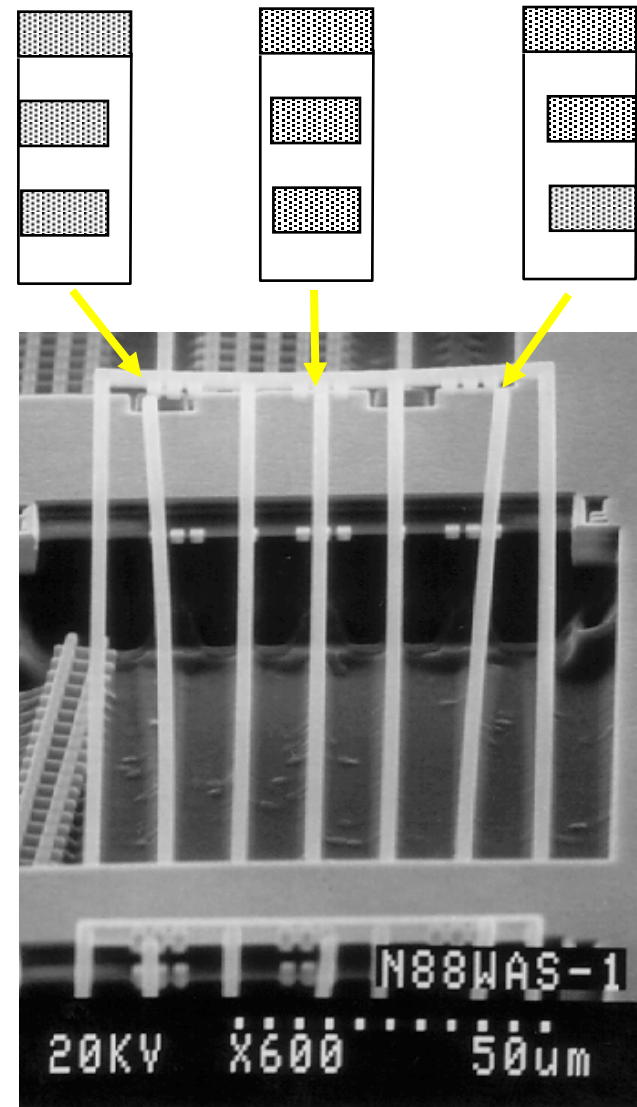
M-TEST P.M. Osterberg, S.D. Senturia, JMEMS '97

- Pull-in of cantilevers, fixed beams and diaphragms
- Electrical test to extract E and tensile σ
- Challenge to generalize and be accurate
- e.g., compressive σ , stress gradients, support compliance, substrate curvature



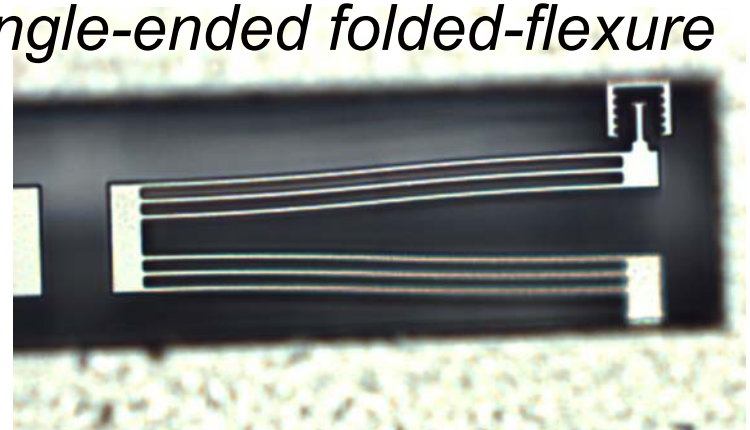
Lateral Curl Example

- Metal offset creates lateral stress gradient
- Direction of curl depends on CMOS misalignment
- SEM shown is Agilent 0.5 μm CMOS
 - 100 μm -long, 1.2 μm -wide beams
 - 0.3 μm offsets of metal-2 and metal-1 with respect to metal-3



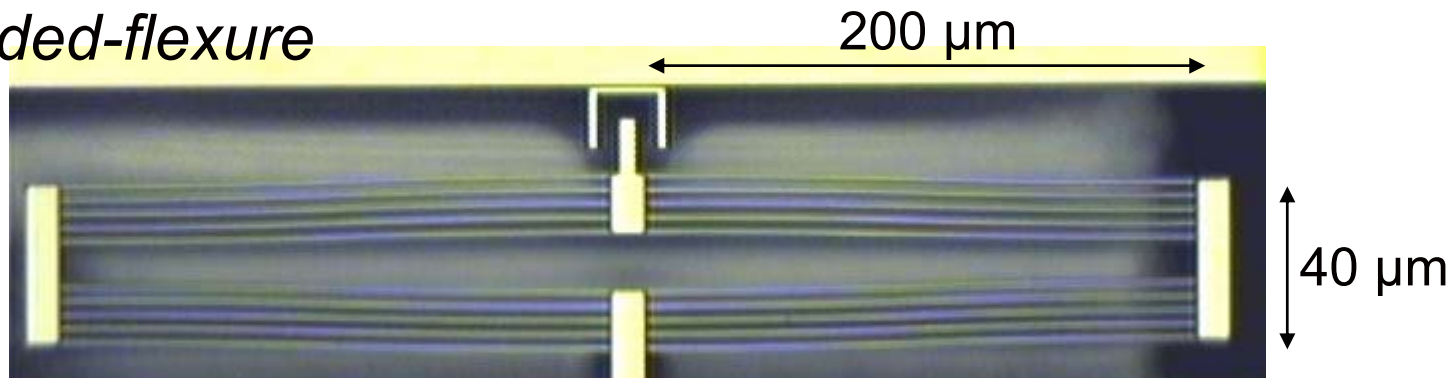
Actuator Operation

- Stiff actuators made with beams *single-ended folded-flexure* in parallel (e.g. 5 beams)
- $40 \times 200 \mu\text{m}^2$ actuator provides up to $25 \mu\text{m}$ stroke (7.5 mW) and 1.2 ms response

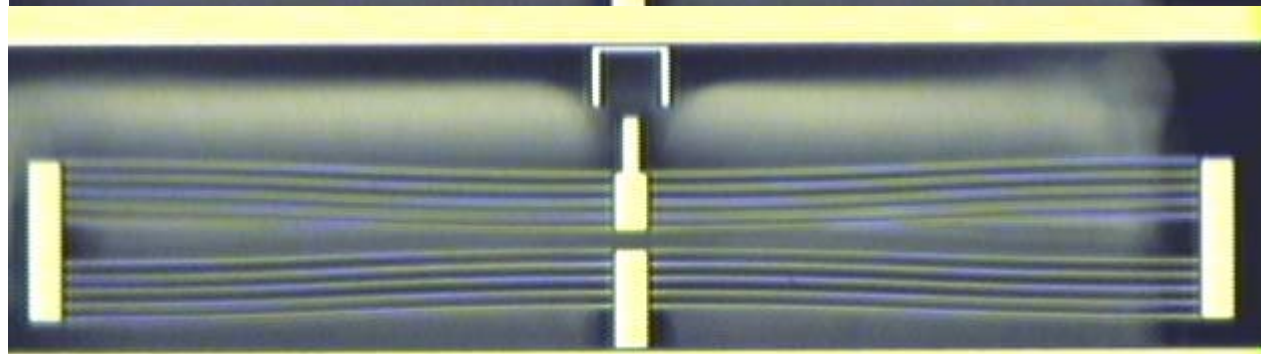


symmetric folded-flexure

10 μm self
actuation
(25°C)

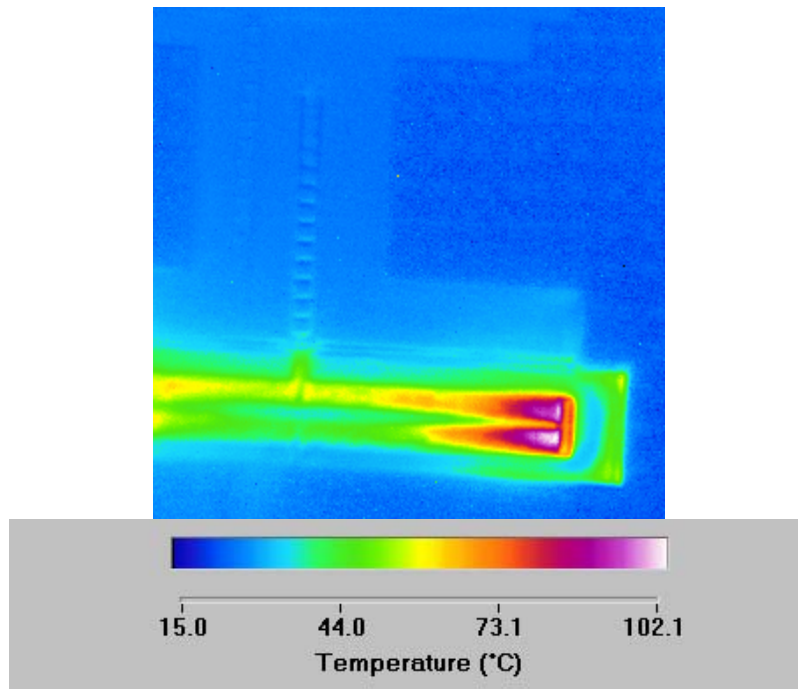


20 μm
electrothermal
actuation
(178°C)



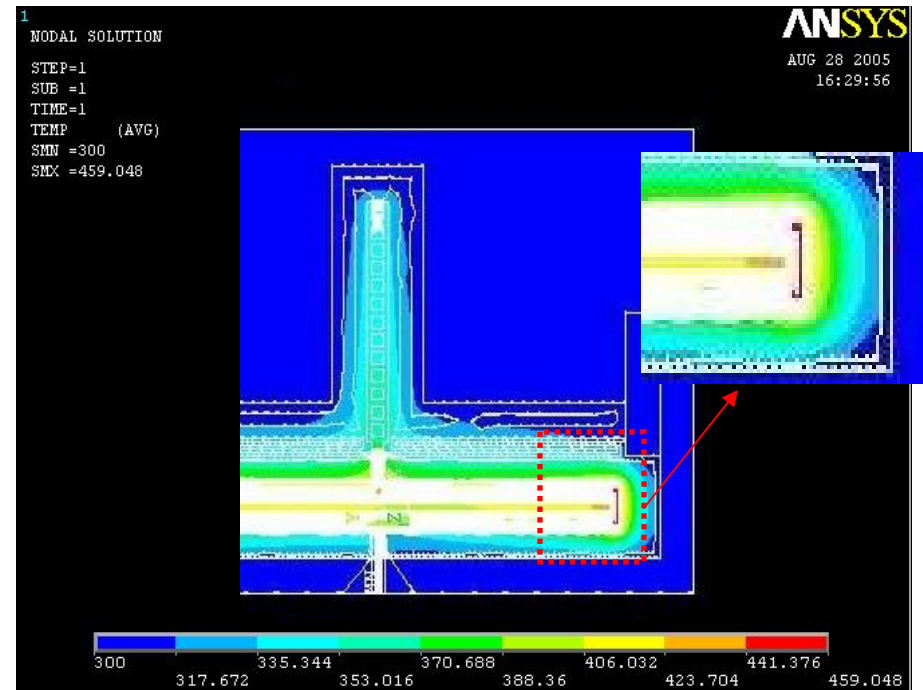
Electrothermal Lateral Actuator (Temperature Distribution)

Measurement:



maximum $T = 375K$

Simulation:



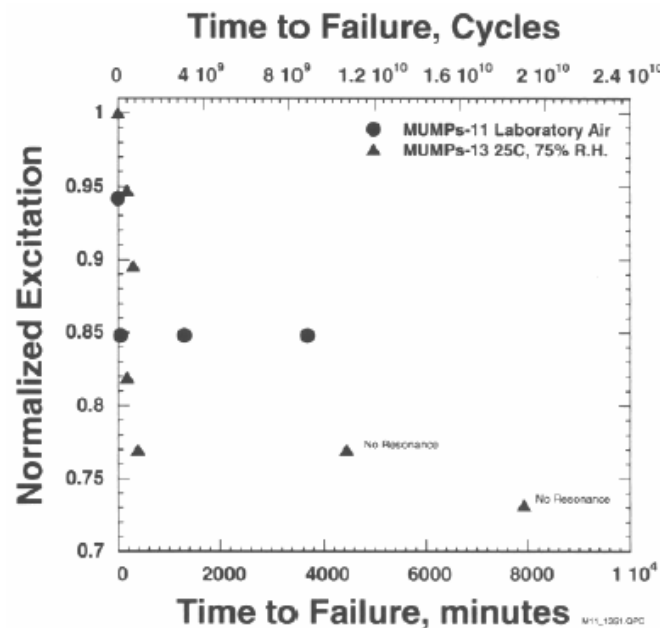
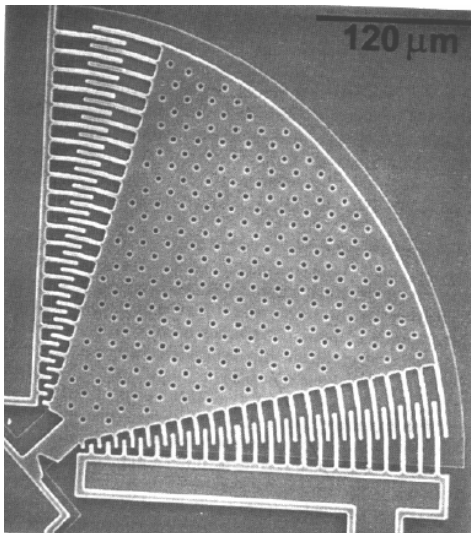
maximum $T = 459K$

- *Driving voltage = 2.5V*
- *Background temperature is set to 300K*

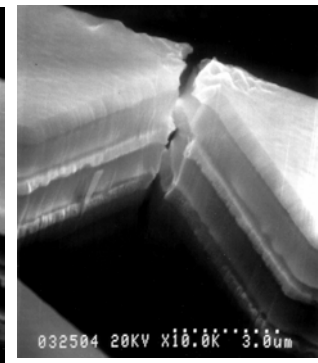
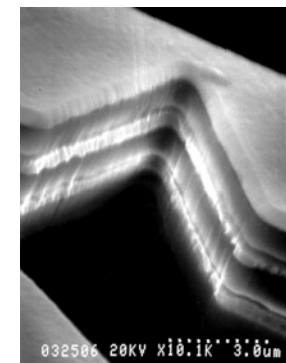
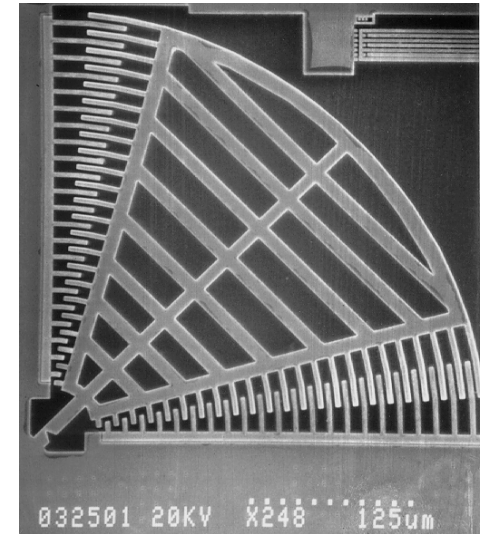
Cyclic Fatigue

- “Notch” structure first presented by Failure Analysis Associates and MIT
- Studies few and far between..
- Dependent on ambient

polysilicon example:



CMOS-MEMS accelerated fatigue example,
M. Lu et al, MRS, 1998

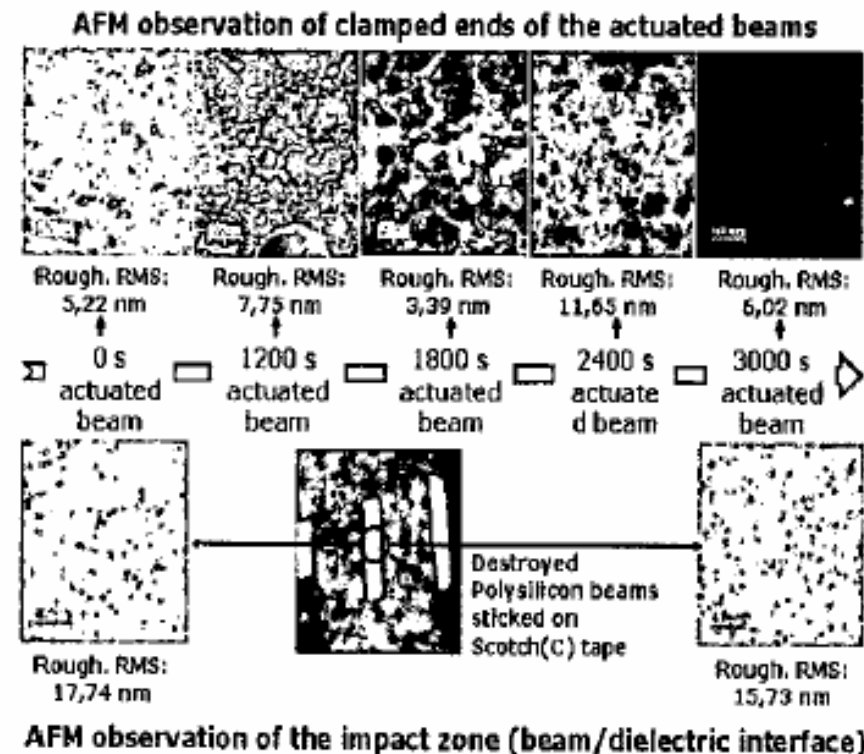
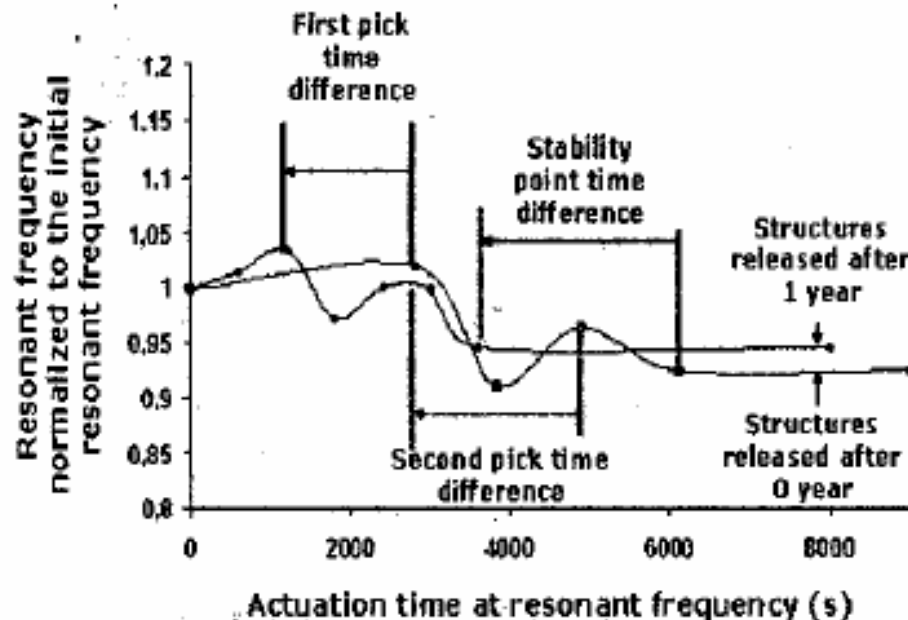


4.5 million cycles, 10 μm stroke, 620 MPa

C. Muhlstein et al, Tribology Issues and Opportunities for MEMS, B.Bhushan, 1997

Material Property Changes with Fatigue

- Polysilicon grain dilatation with cyclic stress
- Two-peak resonant frequency profile with time
- Aged structures stabilize faster

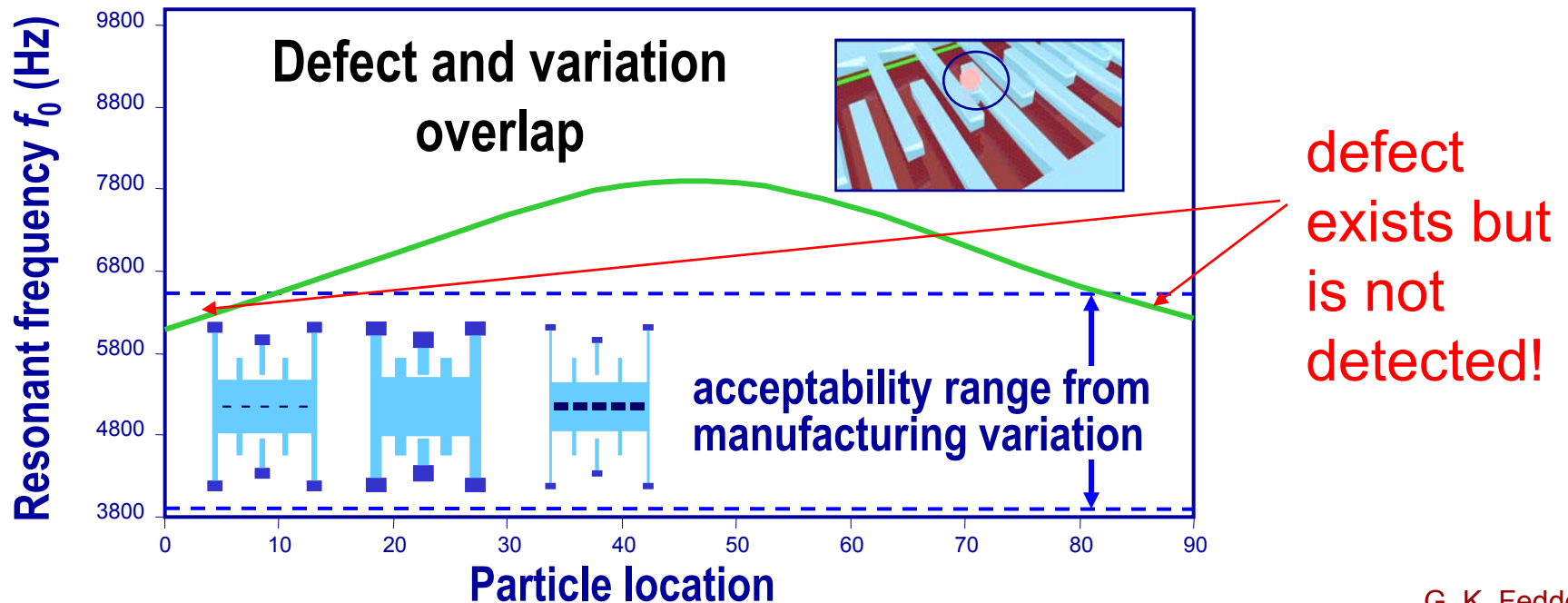
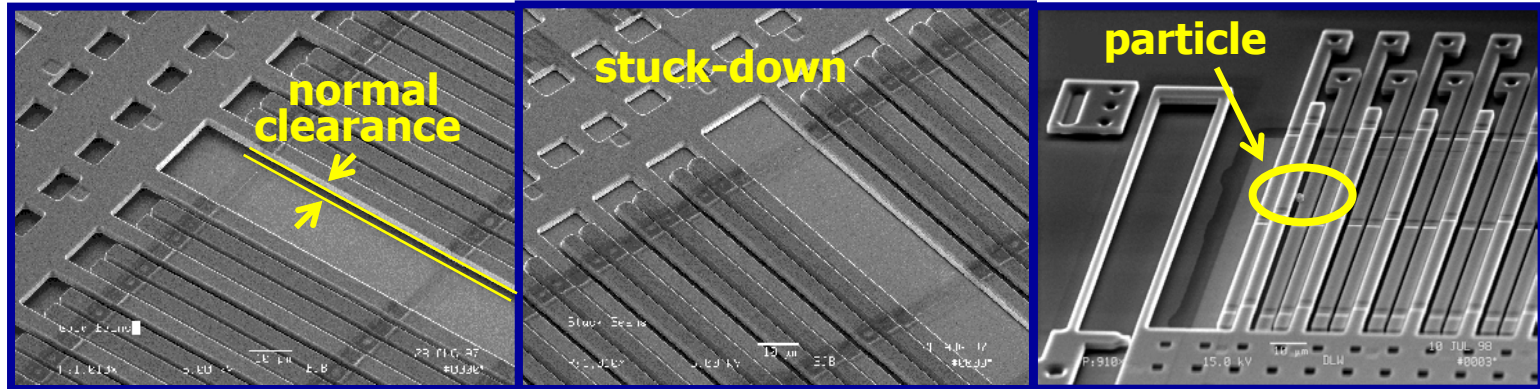


MEMS Fault Testing

R.D. Blanton, Carnegie Mellon

■ Specification-Base Test for MEMS Defects Insufficient

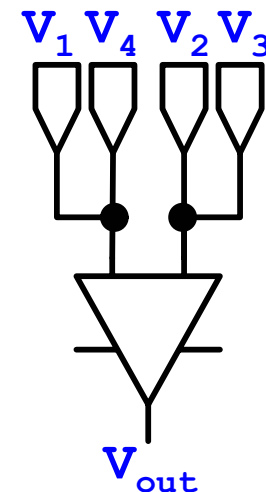
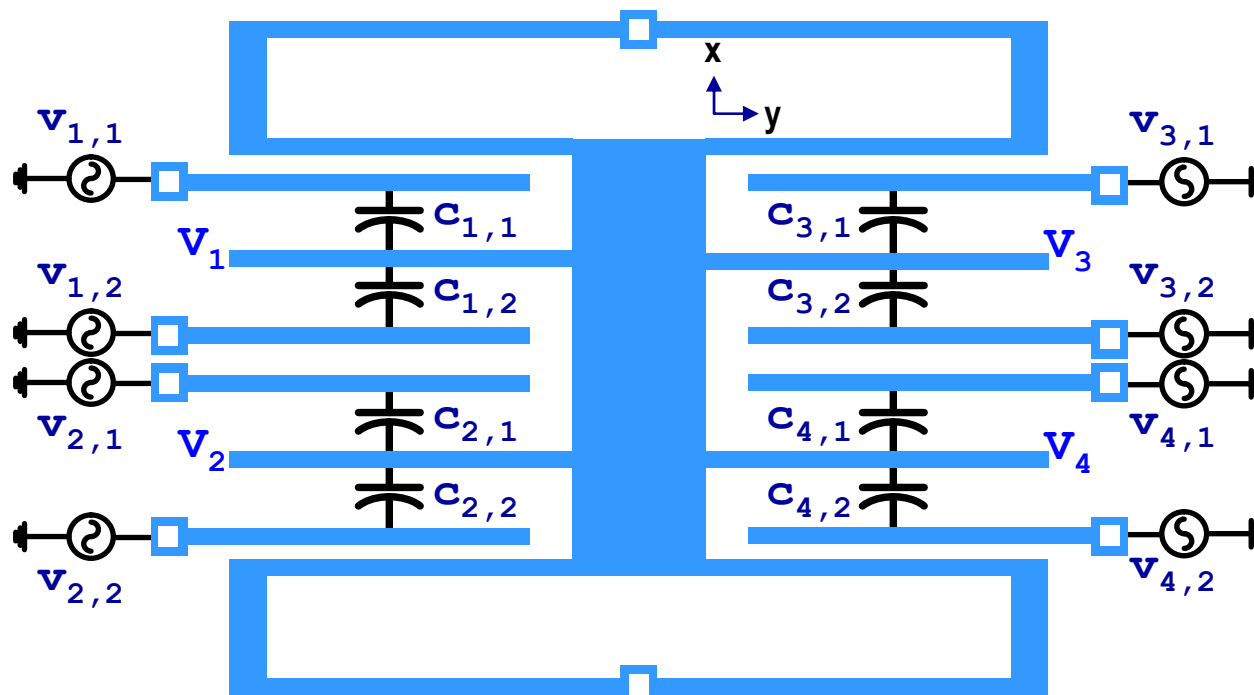
ADI accelerometer example



Accelerometer Built-In Self-Test (BIST)

*R.D. Blanton,
Carnegie Mellon*

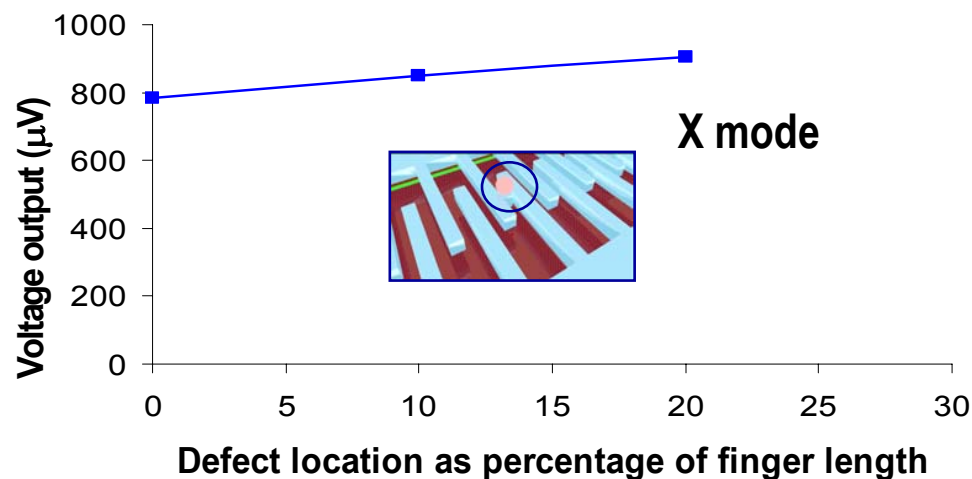
■ Multi-mode actuation to identify faults



pos: $V_{i,1}=V^+$; $V_{i,2}=V^-$

neg: $V_{i,1}=V^-$; $V_{i,2}=V^+$

Normal	1:pos 4:pos 2:neg 3:neg
X mode	1:pos 4:neg 2:neg 3:pos
Y mode	1:pos 4:neg 2:pos 3:neg
X and Y	1:pos 4:pos 2:pos 3:pos



The Case for Built-In Self-Test (or “Self-Assessment”)

- BIST is needed for defect detection and diagnosis
- BIST however can also be used in the field during the lifetime of the design as a "reliability" watchdog or checker
- BIST also can be used for process characterization in the context of the given system
 - standard test structures *lack* the geometric richness that you find in real designs
 - using BIST measures along with appropriate model(s), allows one to keep track of the process over time with very fine granularity

Conclusions

- **Great need for more automated metrology tools and techniques**
 - **Analysis of variation, faults and reliability require lots of testing**
- **Mechanisms should be employed to encode best practices and design knowledge**
 - **e.g. test structures with analysis equations**
 - **widely adopted, not proprietary**
- **Future may lead to more built-in self-test in production MNT systems**